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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,283	08/27/2003	Takayuki Kitazawa	031080	4445

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP  
1250 CONNECTICUT AVENUE, NW  
SUITE 700  
WASHINGTON, DC 20036

EXAMINER
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RUTLAND WALLIS, MICHAEL

ART UNIT	PAPER NUMBER
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2836

MAIL DATE	DELIVERY MODE
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06/18/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/648,283

Applicant(s)

KITAZAWA ET AL.

Examiner

Michael Rutland-Wallis

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2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 26 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-22 is/are pending in the application.
- 4a) Of the above claim(s) 16 and 17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1,3-15 and 18-22 is/are rejected.
- 7) ☐ Claim(s) 4-6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments, filed 04/26/2007, have been fully considered and are persuasive. The previous rejections and objections have been withdrawn. However, upon further consideration, a new ground of rejection is made below.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -  
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1, 3, 7, 10-12, 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Kohama et al. (U.S. Pat. No. 5,731,607)

With respect to claims 1 and 18 Kohama teaches a switching circuit (Fig. 8) comprising: switching transistors (FETs 14 and 15) commonly connected to a connection node (node intersecting or between FETS 14, 15) used as a high frequency signal input/output terminal (when shunt transistor 16 is conducting see connections via R9 and R11 in input output terminals RF11 and RF13) of the switching circuit (14); and a control bias supply circuit (Vdd2) that supplies a control bias for cutting off all the

switching transistors (FETs 14 and 15) to the switching transistors in order to prevent (improve isolation col. 4 lines 40-45) high frequency signal (RF signal described in col. 1 as 1.9 and 1.66 GHz) from substantially propagating (propagating from RF1 to RF2) through all the switching transistors when all of the switching transistors are in a non-selected state (when signal path from RF14 to RF 15 is not selected) in which all the switching transistors are turned OFF in response to selection control signals (CTL1 and CTL 2) applied to gates of all the switching transistors (11 and 12).

With respect to claim 3 Kohama teaches the control bias supply circuit supplies the control bias in accordance with a voltage signal that is applied from outside of the switching circuit (i.e. not seen in switch circuit 11 in Fig. 5).

With respect to claim 7 Kohama teaches the control bias supply circuit varies a voltage value (from high to low to control the conduction of the FETs 11 and 12) of the control bias.

With respect to claim 11 Kohama teaches at least three switching transistors, which are commonly connected (See Fig. 5)

With respect to claim 12 Kohama teaches a shunt transistors (FET13) respectively provided for the switching transistors and are connected between the connection node and a given potential, gates of the shut transistors receiving the select control signals.

With respect to claims 10 and 22 Kohama teaches supplying the control bias having a first voltage value (ON voltage) when at least one of the switching transistors is in a selected state and supplying the control bias having a second voltage (off voltage)

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value different from the first voltage value when all the switching transistors are in the non-selected state.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-9, 13, 19 and 20-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Kohama et al. (U.S. Pat. No. 5,731,607) in view of Matsunaga et al. (U.S. Pub. No. 20030016082)

With respect to claims 8-9 and 20-21 Kohama teaches the device of claim 1 as understood by the examiner, however Kohama does not teach the control bias varies the control voltage of the control bias circuitry when the switching circuits are in a non-selected states. Matsunaga teaches the use of a control bias circuit, which teaches the capability of varying the voltage, supplied the voltage control terminals of switching transistors. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kohama to use a control bias circuit similar to that seen in Matsunaga in order to prevent excess current flow to the switching transistors.

With respect to claims 13 and 19 Kohama teaches the device of claim 1. Kohama does not teach the use of MESFET in the control bias supply circuit. Matsunaga teaches the use of transistors in the bias control circuitry if it is held no transistors are to be connected to the control terminal of Kohama. Kohama teaches the use of FETs. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a MESFET over another type of FET to increase the switching speed

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohama et al. (U.S. Pat. No. 5,731,607) in view of Ayasli et al. (U.S. Pat. No. 5,012,123) Kohama does not teach ballast resistors, each of which is connected between a source and a drain of a corresponding one of the switching transistors. Ayasli teaches the use of ballast resistors see fig 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to in order to establish a biasing voltage source and drain of the switching transistor.

### ***Allowable Subject Matter***

Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 4 Kohama teaches the switching circuit of claim 1 however does not teach the control bias supply circuit comprises a diode having an anode to

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which the voltage signal is applied and a cathode via which the control bias is output to the connection node. At least this further limitation to claim 1 is not taught or rendered obvious by the prior art of record.

With respect to claims 5 and 6 Kohama teaches the switching circuit of claim 1 however does not teach control bias supply circuit comprises a bias transistor including a structure of a MESFET; and the MESFET having a gate receiving a voltage signal, a first terminal connected to a given potential via a capacitive element, and a second terminal connected to the connection node, the control bias being supplied to the connection node from the second terminal. At least this further limitation to claim 1 is not taught or rendered obvious by the prior art of record.

### ***Conclusion***

Applicant's amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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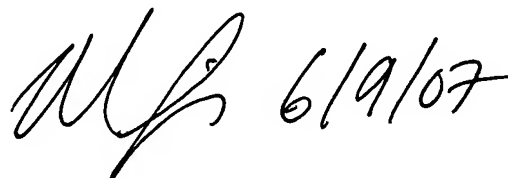
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MRW



MICHAEL SHERRY  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800